

# AccuBridge™ TOWARDS THE DEVELOPMENT OF A DC CURRENT COMPARATOR RATIO STANDARD

Duane Brown<sup>1</sup>, Andrew Wachowicz<sup>2</sup>, Dr. Shiping Huang<sup>3</sup>

<sup>1</sup>Measurements International, Prescott Canada [duanebrown@mintl.com](mailto:duanebrown@mintl.com), <sup>2</sup>Measurements International, Prescott Canada [mieng1@mintl.com](mailto:mieng1@mintl.com), <sup>3</sup>Dr. Shiping Huang [mieng4@mintl.com](mailto:mieng4@mintl.com)

## ABSTRACT

Inherent ratio errors of 0.1 to 0.2ppm in the Direct Current Comparator (DCC) have hindered its development as a standalone bridge. By improving the technologies described in the paper, the reduction of the inherent ratio error of less than 0.02ppm can be achieved. Verification of the ratio accuracy can now be performed from a ratio of 0.07:1 to 14:1 with a resolution of 0.001. Automatic balancing facilitates the operation of the bridge for more accurate resistance measurements over the range of 0.1Ω to 100kΩ.

Key Words: Direct Current Comparator (DCC), ratio error, improved partial turn technology, ampere turns, and variable slave turns, turns calibration.

## 1. INTRODUCTION

The DCC is an ampere turn device consisting of the master turns ( $N_x$ ) and slave turn ( $N_s$ ), shown in Figure 1.

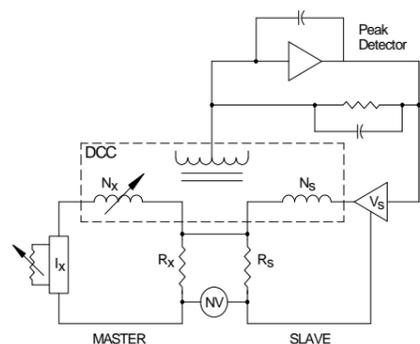


Figure 1 Conventional Ratio Bridge Block Diagram

The DCC, wound in decimal format, had 11,111 master turns and a 1000 turn slave winding where the master turns include both real and partial turns. When the DCC is at balance,

$$I_x \cdot N_x = I_s \cdot N_s \quad (1)$$

A current source is used for supplying the master current and a voltage source for the slave current. This

technology has been in service for 40 years, working at the 0.1 to 0.2 ppm accuracy level for ratios of 1:1 to 10:1. Accuracy in this technology was limited due to the loading effect of the partial turns on the current splitting resistor, the temperature coefficient of the wire used to construct the fractional turns and the noise level created by the modulation frequency which was fed through to the nanovolt detector. There was no real way of using the technology to verify the accuracy claimed on the technology. Resolution was limited to 0.1ppm for 1:1 ratios, 0.01ppm for 10:1 ratios and 1ppm for 0.1 ratios.

Ratio verification of the DCC could be performed using the interchange technique for 1:1 ratios as in Equation 2,

$$r_e = (R_f - \frac{1}{R_r})/2 \quad (2)$$

$r_e$  and  $R_f$  and  $R_r$  represented as the interchange error, forward ratio and reversed ratio *respectively*. However, for ratios of 1:10 (0.1 ratio), the interchange technique could not be used within the accuracy claimed as the master turns were reduced from 10,000 to 100 turns, reducing the ampere turn sensitivity of the measurement by 100 and increasing the interchange error from 0.1 ppm to 1 ppm. And due to the limited number of turns, flux distribution or flux leakage would not be as uniform for a 0.1 ratio as compared to a 1:1 or 10:1 ratio measurement.

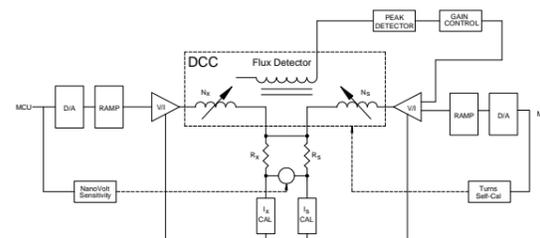


Figure 2 AccuBridge™ Block Diagram

The AccuBridge™ technology shown in Figure 2 uses a binary wound comparator for both variable master and slave turns. An unloading circuit is used to unload the resistance of the partial turns from the current splitting resistor. A new peak (flux) detector with increased sensitivity provides more stable and increased gain by

removing the modulation frequency from the voltage detector for quieter measurements.

Master and slave current tracking has a direct influence on the bridge accuracy by two types of the gain and hysteresis.

Gain error is coming mostly from the turn error. The turn's calibration for AccuBridge™ is used to diagnose the deviation of each winding and to provide a way for determining the ratio correction.

Hysteresis error is hard to numerical estimation. It comes from changes of the residual flux in the DCC shield, created during current transients (like preliminary measurements, turn changes under bias, or current reversals). It was measured to create interchange error in the range of 0.1ppm – 0.4ppm at both 1:1 and 10:1 ratios. The errors can be reduced down significantly by making both tracking sources with the ramping translation.

The self-calibrating and linear-ramping current sources are used to switch the current on both the master and slave and to demagnetize the cores during current reversal. The slave current source is a mirror of the master current source and is integrated with a feedback path from the flux detector. The AC response path has been eliminated decreasing the alternating components at the output of the peak detector to lower the overall noise level present in the comparator and voltage detector.

The nanovolt sensitivity feature determines an accurate overall gain for measuring the differential input to the nanovolt detector (board), related to the equivalent turn's changes.

## 2. DESIGN STRATEGIES

### 2.1 Ramping sources for reducing interchange errors

Both the master and slave sources are controlled using 16-bit digital-to-analog converters with a specific integrated circuitry to perform the required ramping feature. The generic block diagram is given in Figure 3, where resistor, R, and capacitor, C are used to adjust the required ramping timing during the currents are reversed. The master source has the capability of calibrating the current source to within 100ppm.

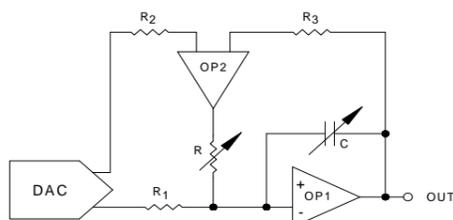


Figure 3 Ramping Source Block Diagram

### 2.2 Unloading circuit for omitting the effects over the winding resistance of the DCC partial turns

Unloading circuit is capable of keeping the split current flowing through the partial turn (PT) windings from the variable resistances of the partial windings and relays. The principle is shown in Figure 4. The split current,  $I_{spt}$  becomes a constant current source controlled only by the master current  $I_x$  with 1/128 scale, as given in Equation 3. A generic circuit to implement the precision splitting function has been build, shown in Figure 5 with a lower noise isolated power supply, to verify the unloading performance and capability of the drive.

$$I_{spt} = \frac{I_x}{128} \quad (3)$$

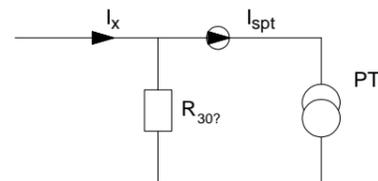


Figure 4 Unloading Diagram

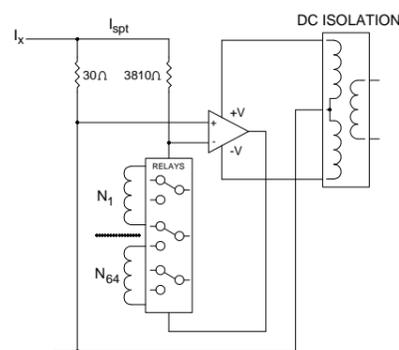


Figure 5 General Block Circuitry

### 2.3 Turns calibration for the DCC's turn alignment

Accuracy of the DCC bridge depends first of all on accuracy and stability of the DCC windings. There are two kinds of winding inaccuracy: uncorrected number of the turn on a section and an additional, parasitic magnetic coupling to the core, effect causing the equivalent number of turns not to be an integer.

Missing or additional turn on a section is easily detectable and corrected during transformer manufacturing. Parasitic magnetic coupling is very small, difficult to measure and was typically neglected. So the contributed error may be in an order of  $10^{-8}$  (0.01ppm) or higher and could limit accuracy of the bridge.

A self-calibration procedure, for obtaining the deviation

of the individual turns, adds the errors in the compensation procedure for the ratio corrections. The basic concept is to connect a set of windings in series, some of them in forward or reverse direction, pass a test current and measure the resulting magnetic flux in the DCC. When the numbers of turns in the forward and reverse directions are exactly equal, the resulting flux should be zero. Otherwise, the non-zero reading is the error of the winding. The process starts from using a reference winding 2048 turns ( $2^K=2^{11}$ ), which is compared to others in the same number but in the opposite direction. Then the process is carried out step by step, including the slave turns, down to 1 real turn ( $2^0$ ) and end in the partial turns. The process is able to measure the errors of each winding, and described in details below,

Let the real number of turns of each winding be represented as:

$$X_K = N_K + \Delta N_K \quad (4)$$

Where:

$N_K$  – the  $K$ th ideal number of turns;

$\Delta N_K$  – the  $K$ th turns error;

Each calibration step compares number of turns:

$$X_K - X_{(K-1)} - X_{(K-2)} - \dots - X_1 - X_{1E} = m_k \quad (5)$$

Where:

$m_k$  – measurement result expressed in number of turns.

$N_{1E}$  – an extra one turn for calibration test

Flux detector is calibrated in ampere-turns. Measurement result has to be normalized to take into account test current and number of turns

$$m_k = \frac{FD_K}{I_K} \quad (6)$$

Where:

$FD_K$  – Flux detector reading in ampere-turns [AT];

$I_K$  – Test Current;

By definition, the ideal turns would compensate and produce output equal to zero, therefore (5) becomes:

$$\Delta N_K - \Delta N_{(K-1)} - \Delta N_{(K-2)} - \dots - \Delta N_1 - \Delta N_{1E} = m_k \quad (7)$$

Assume the calibration process using winding 2048 turns ( $2^K=2^{11}$ ) as a reference, the set of the equations (at  $K=11, 10\dots 0$ ) is given in Equation (8), derived by Equation (7).

$$\Delta N_{2^k} - \sum_{p=1}^K \Delta N_{2^{(k-p)}} - \Delta N_{1E} = m_{2^k} \quad (K=11 \dots 1, 0) \quad (8)$$

By definition, winding 2048 turns is used as a reference, given by

$$\Delta N_{2048} = 0 \quad (9)$$

From Equation (8), two equations for 2048 ( $K=11$ ) and 1024 ( $K=10$ ) turns can be obtained by

$$\Delta N_{2048} - \Delta N_{1024} - \Delta N_{512} - \dots - \Delta N_1 - \Delta N_{1E} = m_{2048} \quad (10)$$

$$\Delta N_{1024} - \Delta N_{512} - \Delta N_{256} - \dots - \Delta N_1 - \Delta N_{1E} = m_{1024} \quad (11)$$

Subtract Equation (10) to (11) with Equation (9); the error of the 1024 turn can be derived by

$$\Delta N_{1024} = \frac{m_{1024} - m_{2048}}{2} \quad (12)$$

$M_{1024}$  and  $m_{2048}$  are measured and calculated from Equation (6). For  $\Delta N_{512}$ ,  $\Delta N_{256}$  ... and so on to  $\Delta N_1$ , the turn's errors of the turns can be figured out by Equation 13.

$$\Delta N_{2^k} = [2^{(10-k)} \cdot m_{2^k} - \sum_{i=k}^{K \leq 9} 2^{(9-i)} \cdot m_{2^{(i+1)}} - m_{2048}] / 2^{(11-k)} \quad (K=10 \dots 1, 0) \quad (13)$$

Here  $K=10\dots, 0$  is related to the 1024, 512..., 1 number of the turns. Also, the error of extra one turn can be derived by

$$\Delta N_{1E} = -\Delta N_1 \quad (14)$$

The similar procedure is able to calibrate the slave turns; by selecting the any same number of the master turns in the opposite turn starts.

#### 2.4 Nanovolt sensitivity detector for improving ratio errors

Nanovolt amplifier measures the residual voltage at the bridge. It is used to calculate the final resistor ratio, by interpolating between the direct current comparator steps. As 1 partial turn step has an equivalent to about 7.6ppm (1024 turns) at 1:1 ratio, 1.5 ppm (5120 turns) at 10:1 ratio and 76ppm at 1:10 ratio.

Accuracy of the interpolation process depends on absolute accuracy of the measurement, which includes gain of the amplifier, accuracy of the current sources (Master and Slave), as well as accuracy of the A/D converter.

- 0.1% error of the gain of the amplifier gives 0.01ppm error at 1:1 resistor ratio. It gives about 0.0016ppm at 10:1 ratio (5120 turns) and 0.039ppm at 1:10 ratio (204 turns).
- 0.1% error of the Master current source, with the perfectly tracking Slave, gives 0.01ppm error at 1:1 resistor ratio, 0.0016ppm at 10:1 ratio (5120 turns) and 0.1ppm at 1:10 ratio (204 turns).
- Absolute accuracy of the A/D converter depends first of all on the accuracy of the reference source.

The absolute accuracy of ADC with  $\pm\Delta(\text{mV})$  at 2.5V output will give an error of  $\delta=\pm\Delta/2,500(\%)$ . It gives maximum error of  $\delta(\text{ppm})$  at 1:1 ratio,  $0.1\times\delta(\text{ppm})$  at 10:1 and  $10\times\delta(\text{ppm})$  ppm at 1:10 ratio.

- Temperature coefficient of the A/D converter reference is  $30\text{ppm}/^\circ\text{C}$ . Error resulting for  $10^\circ\text{C}$  operating temperature change at 1:1 ratio is 0.003ppm.

Sensitivity (gain) of the nanovolt detector is measured automatically and finely to improve the ratio correction. The process is performed automatically by toggling an extra 1/128 turn ( $\Delta N$ ) to determine the overall gain of the nanovolt detector in the different ranges. The expected voltage is formularized in Equation 15. The DC offset has been removed in the equation by reversing the current.

$$\Delta V = \frac{\Delta N}{N_x} \times R_x \times I_x = \frac{\Delta N}{N_s} \times R_s \times I_x \quad (15)$$

### 2.5 Removal of AC path decreasing modulation noise

When a voltage source is adopted as the slave tracking signal, an AC path needs to use to provide a feedback loop through the DCC for a stability demand. In the AccuBridge™, an AC path has been removed from the peak detector for eliminating the modulation frequency noise through the DCC. An optimized controlling process is used to adapt the initial transient stage.

### 2.6 Variable slave turns for reducing the noise issue

The Slave turns can be automatically selected over the ranges, increasing the ampere turns and reducing the noise in the DCC. The 1:1 ratio measurement could be up to 2048 turns, and the 512 turns are used for above 6.5:1 up to 14:1 ratio.

## 3. SYSTEM DESCRIPTION

System architecture is composed of the initialization, basic operating sequence and self-calibrations for the different purposes and characteristics of the operation, before the measurement is carried out.

- System initialization – including the microprocessor configurations, I/O settings selecting the operating mode, self-calibration for the devices on-chip, such as ADCs performed to remove offset and gain errors in the input channels ;
- ADC devices calibration – the overall errors of the ADC readings including ADC
- Calibration for the sources – both master current and slave current are tuned for each measurement by configuring Digital-to-

Analogue device (DAC) setting via the high-precious resistor sensors.

- Turns self-calibration – to measure and store all of the information for each winding in the DCC for the ratio compensation in the firmware,
- Nanovolt gain calibration and adjustment
- Hardware functionalities includes the ramping sources for both master and slave current, tuning the slave DC-offset and the unloading DCC's partial turns.

The System architecture is illustrated in Figure 6, as detailed from Figure 2, in the flowchart for both software (firmware) and hardware implement.

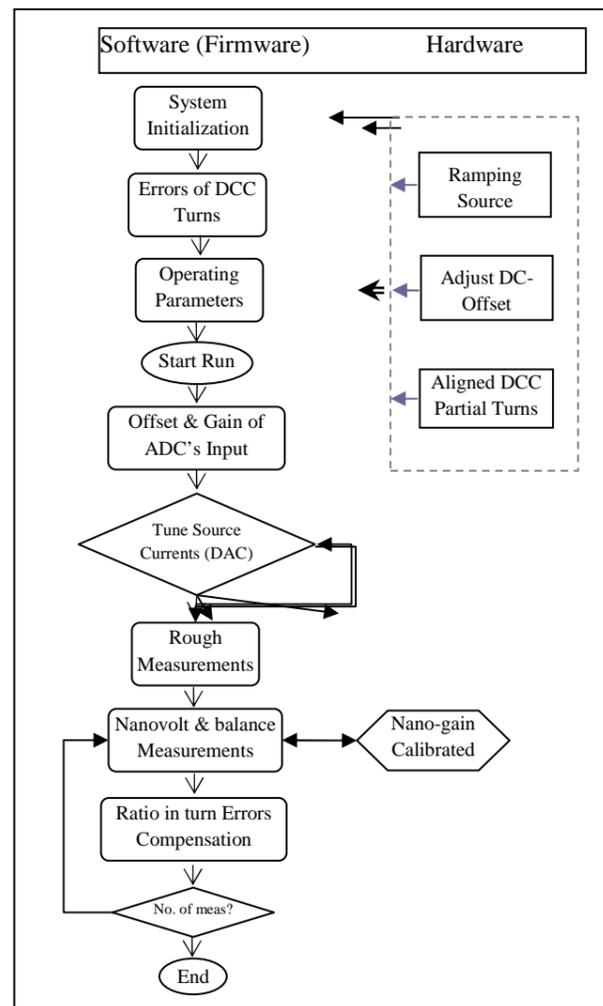


Figure 6 System Architecture Flowchart

## 4. UNCERTAINTY

Although the bridge has performed well by using the several achievements described above, still some rooms are left with the uncertainty field for the further investigations and development.

- A contribution has been made using the linear ramping sources to eliminate the residual flux in the DCC

during the operation and resulted in lower interchange errors significantly. To eliminate the effects of the DCC hysteresis, an study is carrying out if the performance gets better by using the non-linear ramping;

- The levels of the ramping overshoot signal depend on the loads and the number of the DCC turns. The effects could be eliminated in the firmware with the related hardware modification, but may be more complicated;
- In the self-calibration, the 2048 turn is used as the reference to be supposed to be of a lower uncertainty and higher accuracy of the measurement in the high number of the turn. The accumulated errors need to be evaluated for the complete procedure with highest turn (2048), or lowest turn (1) or middle turn (512 slave)
- The sensitivity of the peak detector in DCC is one of the important parameters for the stability, transient procedure and minimum setting timing and so on. To determine the proper and various value for the different loads and number of the turns may be a challenge study.

### TEST RESULTS

Three prototypes have been built and tested for ratio error and standard deviation measurements using the interchange technique. A 1:1 ratio measurement is listed in Table 1. For 10:1 measurements, the AccoBridge™ principle was compared to a calibrated bridge, errors and standard deviation are shown in Table 2. Table 3 represented the results of the interchange errors and standard deviations at 10:1 and 1:10 ratios. Thirty-five (35) measurements are made with the last twenty-five (25) statistics and a 12s setting time.

**Table 1** 1:1 Ratio Interchange Measurements

Rx:Rs(ohm)	Ix(mA)	Measured Ratio	Dev(ppm)	Inter_error(ppm)
1:1	31.6	1.000042417	0.01	0.005
		0.999957595	0.00	
10:10	10.0	0.999996134	0.00	-0.002
		1.000003863	0.00	
100:100	3.0	1.000021302	0.00	-0.002
		0.999978694	0.00	
1k:1k	2.0	1.000119479	0.01	-0.009
		0.999880517	0.01	
10k:10k	0.1	0.999571559	0.01	0.028
		1.000428681	0.01	

**Table 2** Ratio Measurements

Rx:Rs (ohm)	Ix (mA)	Calibrated Ratio	Measured Ratio	Dev (ppm)	Erro (ppm)
10:1	5.0	10.00616188	10.00616160	0.002	-0.03
100:10	3.0	9.99346977	9.99346953	0.003	-0.02
1k:100	2.0	10.00020757	10.00020727	0.005	-0.03
10k:1k	0.3	9.99984155	9.99984139	0.002	-0.02

**Table 3** 10:1 Ratio Interchange Measurements

Rx:Rs(ohm)	Ix(mA)	Measured	Dev(pp)	Inter_error(ppm)
10:1	5.0	10.00032980	0.011	-0.021
1:10	50.0	0.09999670	0.013	
25:10	4.0	2.50278105	0.012	0.005
10:25	40.0	0.39955553	0.002	
100:10	3.0	9.99922491	0.008	0.003
10:100	30.0	0.10000775	0.010	
100:25	2.0	3.99545553	0.005	-0.017
25:100	20.0	0.25028434	0.003	
1k:100	2.0	10.01091214	0.006	-0.018
100:1k	20.0	0.09989099	0.033	
10k:1k	0.3	9.99883350	0.020	-0.016
1k:10k	3.0	0.10001166	0.054	
100k:10k	0.1	9.99017779	0.042	-0.123
10k:100k	1.0	0.10009829	0.255	

### CONCLUSIONS

The accuracy of uncertainty of DCC has been improved using AccuBridge™ technology which can be used as a DC Ratio Standard for resistance calibrations. Optimized calibrated ramping current sources, an unloading structure on the partial turns and the self-calibrated alignment of the comparator have improved the technology significantly. The standard deviation of the measurements was significantly reduced by removing the modulation frequency from the peak detector and increasing ampere turns for 1:10 measurements. The technology is suitable for measuring 1:1 ratios with a ratio accuracy of 0.01ppm and <0.02ppm for 10:1 ratios and with slightly reduced accuracy at 10kΩ to 100kΩ. The noise level in all cases was less than the quoted standard deviation of <0.02ppm, from 1Ω to 10kΩ.

The bridge has been in development for about 2 years for the measurement of decade resistors. It is easy to use the IEEE488 interface making it ideal for recording the measurements runs. However, further investigation is required to improve the accuracy for the 10kΩ to 100kΩ ratio. The performance of AccuBridge™ still needs to be verified against the CCC in the NRC National Laboratory. The uncertainty of the bridge will be investigated and reduced for the optimised operation in all of the ranges.

### REFERENCES

- MacMartin and N.L. Kusters, "A direct-current-comparator ratio bridge for four-terminal resistance measurements," IEEE Trans. Instrum. Meas., vol. IM-15, pp. 212-220, December 1966
- MacMartin and N.L. Kusters, "A direct current comparator bridge for high resistance measurements", IEEE Trans. Instrum. Meas., vol IM-22,pp. 382 – 386, December 1973